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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	Not assigned yet 10/796,023
			Filing Date	On even date herewith 3/10/2004
			First Named Inventor	K. ITOH, et al.
			Art Unit	Not assigned yet 2818
			Examiner Name	Not assigned yet
Sheet 1 of 1	Attorney Docket Number		520.40847CC2	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
E		4 771 323		09/88	Sasaki, Masavoshi	Z
		4 920 391		04/90	Uchida, Hidetsugu	
		5 675 160		10/97	Oikawa, Ryuichi	
		6 314 017		11/01	Emori et al.	
		6 388 934		05/02	Tobita, Youichi	
		6 452 858		09/02	Hanzawa et al.	
		6 515 892		02/03	Itoh et al.	
		6 515 195		02/03	Kanno et al.	

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					
E		JP 1-255269 A		10/89			
		JP 63-18847 A		0/88			
		JP 8-250673 A		09/96			
		JP 2-54572 A		02/90			
		JP 58-220464 A		12/83			

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
E		Ultra LSI Memories, Baifukan, Nov. 5, 1994, Kiyoo ITOH, pp. 12-15	
E		ISSCC '72, VLSI Memory Chip Design, Kiyoo ITOH, pp. 12-13	

Examiner Signature	<i>Sei Akiyoshi</i>	Date Considered	6/04
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